Amendments To the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1. (original) A modem system for receiving and transmitting signals comprising:

a frequency domain equalizer (FEQ) block being responsive to a frequency channel response for processing the same to generate one or more initial FEQ coefficients (FEQ1), said modem system being responsive to an input signal for processing the same to generate said frequency channel response, said input signal being generated from a transmitted signal, said FEQ block using said FEQ1 to generate an equalized Signal, said modem system demodulating said equalized Signal to generate a demodulated Signal symbol; and

a transmitter responsive to said demodulated Signal symbol for processing the same to generate a remodulated Signal symbol, said modem system for using said remodulated Signal symbol to generate one or more FEQ coefficients (FEQ2), said FEQ coefficients for enhancing the accuracy of said FEQ block in equalizing said frequency channel response,

wherein said FEQ coefficients improve the performance of said modem system by mitigating the effects of multi-path channel arising in transmission of said transmitted signal.

Claim 2. (original) A modem system as recited in claim 1 further including a convolutional decoder, said modem system for using said equalized channel response to generate an encoded equalizer output, said convolutional decoder being responsive to said encoded equalizer output for decoding the same to generate a decoded transmitted signal.

Claim 3. (original) A modem system as recited in claim 2 including an orthogonal frequency division multiplexing (OFDM) receiver, said OFDM receiver for including said FEQ block and said convolutional decoder, said convolutional decoder being a Viterbi decoder, said transmitter being an OFDM transmitter, said input signal for including OFDM-modulated packets.

Claim 4. (original) A modem system as recited in claim3 further including a fast Fourier transformation (FFT) block responsive to an in-coming signal for converting the same from time domain to frequency domain to generate said frequency channel response.

Claim 5. (original) A modem system as recited in claim 4 further including a timing loop and a carrier loop, said input signal for including timing and frequency information used for initializing said timing loop and said carrier loop, said timing loop and said carrier loop for correcting the timing and frequency offsets in said in-coming signal.

Claim 6. (original) A modem system as recited in claim 3 wherein said frequency channel response includes a Signal symbol, said FEQ block processing said Signal symbol using said initial FEQ coefficients to generate said equalized Signal.

Claim 7. (original) A modem system as recited in claim 3 wherein said FEQ block for using said FEQ coefficients for equalizing said frequency channel response to generate an equalized channel response.

Claim 8. (original) A modem system as recited in claim 3 further including a demapper responsive to said equalized channel response for processing the same to generate one or more metric weights.

Claim 9. (original) A modem system as recited in claim 8 further including a weighting block for generating one or more weighted metrics, each of said weighted metrics being generated by dividing said metric weight by the magnitude of said FEQ coefficient, said frequency channel response for including one or more subcarriers, each of said subcarriers being assigned one or more of said weighted metrics, said subcarriers including faded subcarriers, said weighted metrics assigned to said faded subcarriers being substantially small.

Claim 10. (original) A multi-carrier modem receiver system as recited in claim 9 further including a de-interleaving block responsive to said weighted metrics for processing the same to generate a de-interleaved output, said de-interleaving

block for parsing data bits from said subcarriers and positioning said data bits in correct order.

Claim 11. (original) A modem system as recited in claim 10 further including a de-puncturing block responsive to said de-interleaved output for processing the same to generate said encoded equalizer output, said de-puncturing block for inserting removed data bits to re-establish a pattern in said encoded equalizer output.

Claim 12. (original) A modem system as recited in claim 10 for demodulating said equalized Signal by using said demapper, said de-interleaving block and said convolutional decoder, said modem system for demodulating said equalized Signal to generate said demodulated Signal symbol.

Claim 13. (original) A modem system as recited in claim 12 wherein said demodulated Signal symbol includes a parity bit, said FEQ block for allowing correct reception of said parity bit to cause remodulation of said demodulated Signal symbol, said FEQ block for allowing incorrect reception of said parity bit to halt further reception of said input signal.

Claim 14. (original) A modem system as recited in claim 12 wherein said transmitter being responsive to said demodulated Signal symbol, said transmitter for including a convolutional encoder, an interleaver and a mapper for

remodulating said demodulated Signal symbol to generate said remodulated Signal symbol ($\sigma_{remod/demod}$).

Claim 15. (original) A modem system as recited in claim 4 wherein said incoming signal includes 2 sequences T_1 and T_2, said FFT block for processing said T_1 and T_2 to generate $FFT(T_1+T_2)$, said FEQ block for using a symbol $L_{26:26}$ to compute said initial FEQ coefficients according to:

$FEQ1 = (2 \times L_{26:26})/FFT(T_1+T_2)$.

Claim 16. (original) A modem system as recited in claim 15 wherein said FFT block being responsive to a Signal for processing the same to generate a $Signal_{RX}$, said FEQ block for computing said FEQ coefficients (FEQ2) according to:

$FEQ2 = (52 \text{ series of } 1\text{'s} \times 3)/(FFT(T_1+T_2) + \sigma_{demod/remod} \times Signal_{RX})$.

Claim 17. (original) A modem system as recited in claim 3 wherein said FEQ block includes said transmitter.

Claim 18. (original) A method for receiving and transmitting signals comprising:

receiving a frequency channel response for processing the same to generate one or more initial frequency domain equalizer coefficients (FEQ1);

receiving input signal for processing the same to generate the frequency channel response;

using the FEQ1 to generate an equalized Signal;

demodulating the equalized Signal to generate a demodulated Signal symbol;

processing the demodulated Signal symbol to generate a remodulated Signal symbol;

using the remodulated Signal symbol to generate one or more FEQ coefficients (FEQ2) for enhancing the accuracy of frequency channel response equalization.

Claim 19. (original) A modem system for receiving and transmitting signals comprising:

means for receiving a frequency channel response for processing the same to generate one or more initial frequency domain equalizer coefficients (FEQ1);

means for receiving input signal for processing the same to generate the frequency channel response;

means for using the FEQ1 to generate an equalized Signal;

means for demodulating the equalized Signal to generate a demodulated Signal symbol;

means for processing the demodulated Signal symbol to generate a remodulated Signal symbol;

means for using the remodulated Signal symbol to generate one or more FEQ coefficients (FEQ2) for enhancing the accuracy of frequency channel response equalization.

Claim 20. (original) A computer readable medium having stored therein computer readable program code comprising instructions for performing the following steps:

receiving a frequency channel response for processing the same to generate one or more initial frequency domain equalizer coefficients (FEQ1);

receiving input signal for processing the same to generate the frequency channel response;

using the FEQ1 to generate an equalized Signal;

demodulating the equalized Signal to generate a demodulated Signal symbol;

processing the demodulated Signal symbol to generate a remodulated Signal symbol;

using the remodulated Signal symbol to generate one or more FEQ coefficients (FEQ2) for enhancing the accuracy of frequency channel response equalization.